Status of SPADIC

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SPADIC 1.1

Available since 03/2016.

Changes from SPADIC 1.0 → 1.1:

- Updated CBMnet version (no retransmission)
  → stability seems to have improved
- Removal of digital comparator bug
  → confirmed
- Removal of amplifier instability
  → confirmed
- Removal of serializer glitch
  → not quite (see “How to synthesize DDR multiplexers”)[1]

[1] Parallel to this session...

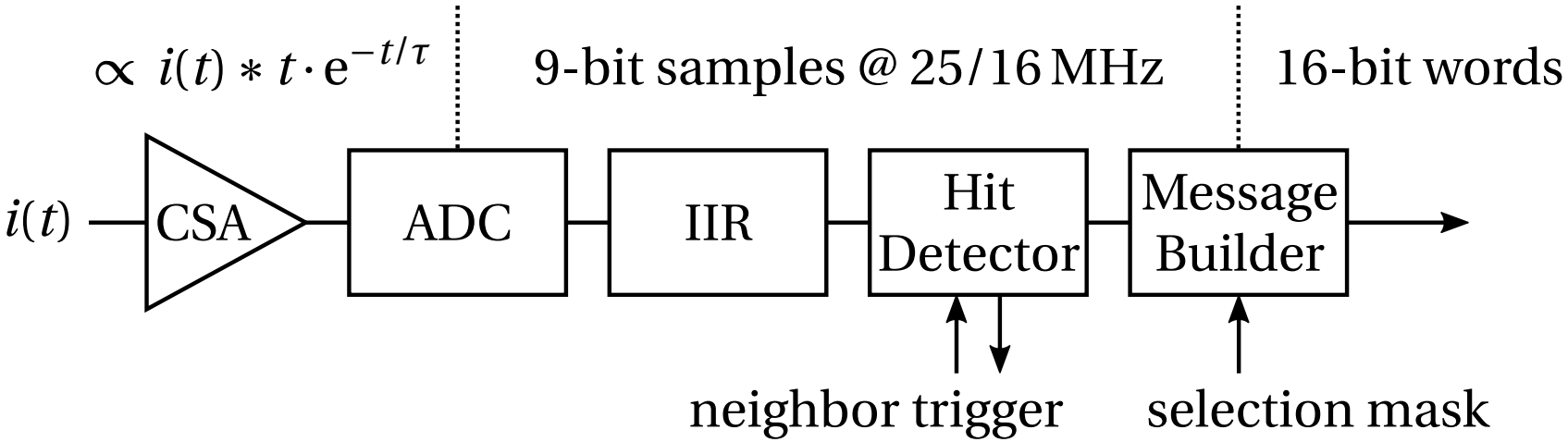
SPADIC 1.1 – FEBs and firmware

- ≈ 50 SPADIC 1.1 chips are available (packaged) – revised FEBs are in production
- Register reading/writing issues reported in 04/2016 are fixed – was a mistake in updating CBMnet from the 1.0 firmware
- Firmwares for Susibo and Syscore3 are available

Section 2

SPADIC 2.0

Reminder – Principle of operation



- 32 channels
- One message contains a recording of the input signal (32 samples)
- Messages from 16 channels merged to time-sorted output stream

Changes in SPADIC 2.0

CBMnet replaced by STS-XYTER protocol

- **Before:** 25 MHz sampling rate, $\tau = 80\,\text{ns} = 2\,T$
  Now: 16 MHz sampling rate, $\tau = 250\,\text{ns} = 4\,T$
- **Before:** Several SPADIC words in one CBMnet packet
  Now: One SPADIC word in one *uplink frame*
- **Before:** CBMnet packet buffers – DLM needed for synchronization
  Now: No buffering – all *frames* intrinsically deterministic – unified configuration and synchonization interface
- Register size changed from 16 to 15 bits – some registers were split
- No triggering of epoch markers needed anymore
- One more “presample”

Using SPADIC 2.0

New FEB needed

- SPADIC 2.0 will be packaged in QFP208 (was QFP176)
- Minor pinout change (new: chip address pins)

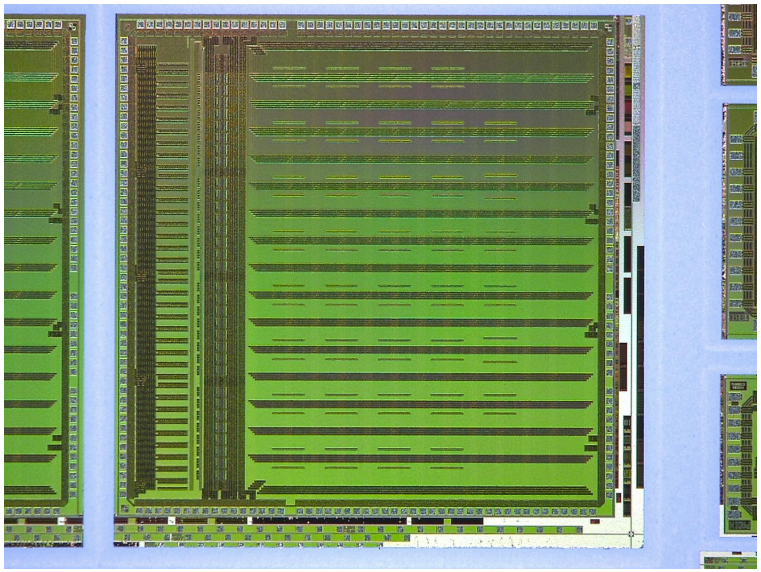
New firmware needed

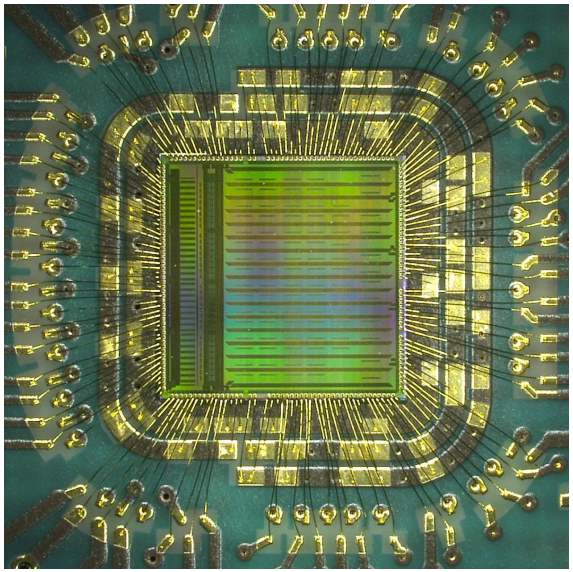
- Implementing the STS-XYTER protocol
- *STS-XYTER tester* can be used as basis

Still the same: one clock (250 → 160 MHz) and one downlink (500 → 160 Mbps), two uplinks (500 → 320 Mbps).
At the abstraction “read/write registers”, “receive message words” and above, nothing has changed.

SPADIC 2.0 availability

- There are two variants of SPADIC 2.0, testing two different implementations of the DDR serializer (in one, the glitch should be gone, but both are usable)
- ≈ 200 chips (packaged) will be available mid October 2016
- ≈ 900 chips (naked) are available now – one of each variant can proably be wire-bonded to SPADIC 1.0 rev.A carrier boards (2 remaining)





Outlook

Revision of data format

- Currently, the STS-XYTER protocol is not efficiently used (one 16-bit word in one 23-bit frame – 7 bits per frame wasted)
- Some of the transmitted data is redundant (e.g. group ID mirrors information already known further “up” in the DAQ chain)
- Investigate more clever ways to reduce the amount of data (e.g. combine data from neighboring channels which belong together anyway)