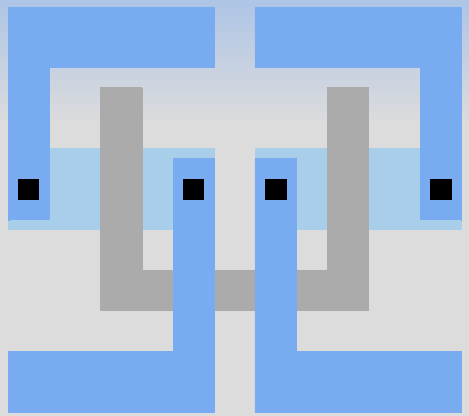
Towards a CBM-XYTER chip



Schaltungstechnik
und Simulation

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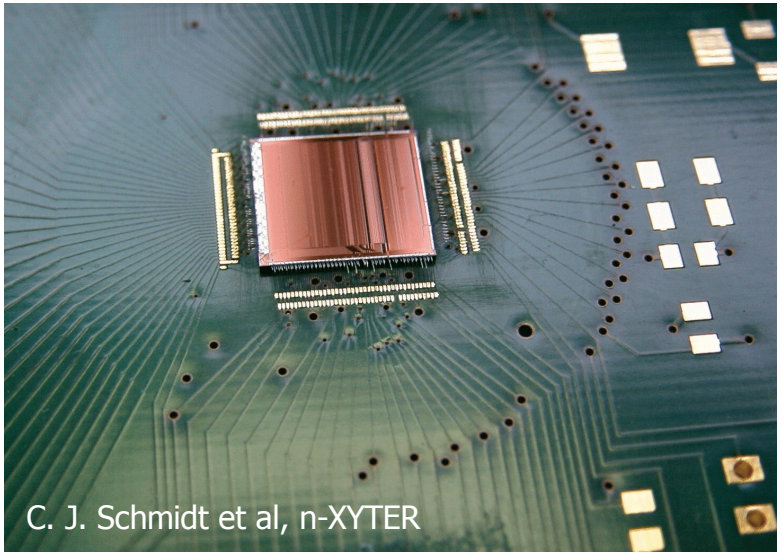
Towards a CBM-XYTER



- The n-XYTER readout chip is being tested for application in CBM
- First n-XYTER measurements are available now
- n-XYTER can be used for first detector tests
- Concurrently, first steps towards the next generation chip 'CBM-XYTER' are made
- Our current aim is to work out specifications & architecture options for CBM-XYTER
- First work packages are already defined but many questions are still open…

Radiation hardness

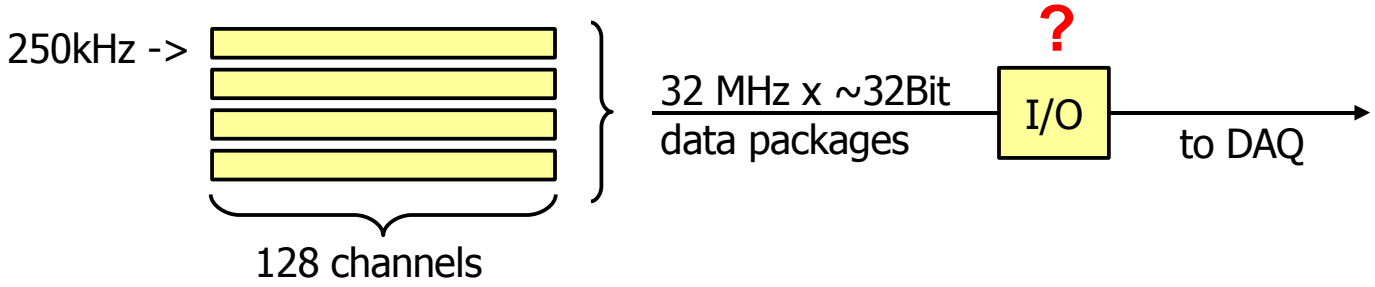
- Baseline technology: UMC018 (most experience in various groups)
- This is certainly rad hard when using special rules. But
  - this costs area = money (~ 4 x in digital part)
  - this costs power (increased caps. ~ 4x in digital part)
  - introduces design limitations (many IPs not usable, no long NMOS, asymmetric characteristics, requires design kit changes,…)
- Question therefore:
  - can we live without special design tricks?

- Possible Design Strategy:
  - Use non-hard standard cells and accept slight increase in leakage current.
  - Use rad-hard layout in critical (small current) analog sections.
- Possible SEU Strategy:
  - Use intrinsically Hamming correcting state machines (Kebschull, Brüning).
  - Use Hamming correction for larger memory blocks.
  - Use SEU 'hardened' cells for single bits (increased capacitance, DICE cell).
  - Generate a parity information from all single bits and send this together with data in a status word to make sure that everything has been ok.
    An error here would trigger a reconfiguration.

Radiation hardness: Workplan

- (HD) Irradiate TRAP chip to high doses (10Mrad)
  - TRAP has already been tested up to 1 Mrad by the ALICE collaboration, in particular Volker Lindenstruth's group
- (MA) Design a digital test-ASIC with identical designs made from
  - radiation hard standard cells
  - non radiation hard standard cells
  - compare power / speed / leakage pre- and post-rad
- (R. Szczygiel, Krakow) Submit Single Transistors for Noise measurements
  - white noise
  - 1/f noise
- (Sven Löchner, GSI) Measure & submit SEU test chips

Data Rates

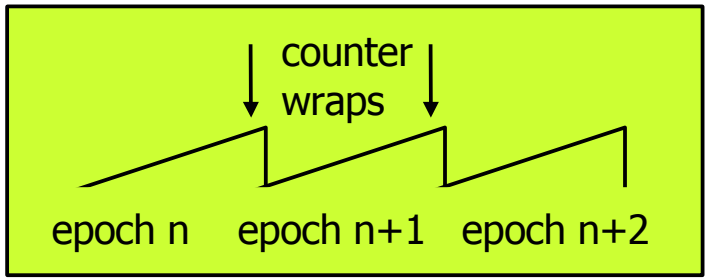


- Hit rate per channel (Poisson): 250kHz → 128 x 250kHz = 32MHz per chip
- Data per hit: ~ 32Bit
  - 10…14Bit time stamp
  - 7 Bit channel id
  - 6…10 Bit Amplitude (assuming ADC)
  - 2..4 Bit Flags
- Total rate per chip: 32Bit x 32MHz = **1 Gbps**

- What physical output channel?
  - LVDS inputs of FPGAs go up to ~600Mbps → 2 links
  - A ~2.4 Gbps high speed I/O building block is planned (Brüning/Tielert) this would give a nice contingency, or we could use one link for two chips

Time stamp/ epoch marker

- At an average hit time difference per chip of ~30ns and a time base clock of 1GHz, average time stamp difference is 30, i.e. 5 Bit.
  Must use 'significantly' more bits than this
- Assume Epoch marker (wrap around flag) is sent at every wrap in a full word:
  - overhead for 8Bit TS: 31ns/256ns = 12%
  - overhead for 10Bit TS: 31ns/1024ns = 3%
  - overhead for 12Bit TS: 31ns/4048ns = 0.7%
- Too long TS increases data volume → 12Bit ?

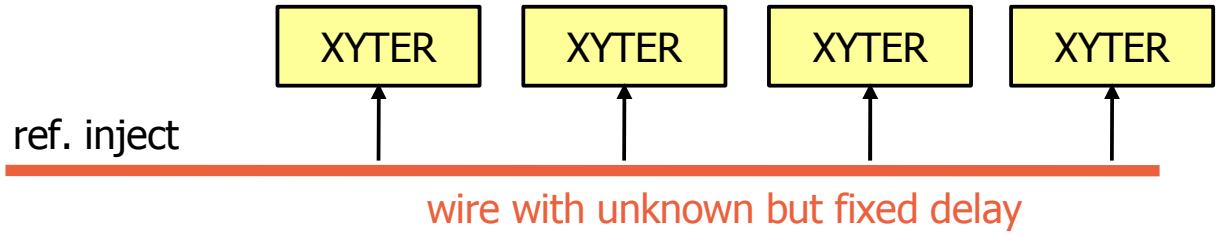


- Is an epoch marker really needed?
  - DAQ detects wrap automatically when enough data arrives.
  - Could inject empty 'dummy' events when one epoch would stay empty.

- Need ideas and detailed simulation of data randomization (Token Ring, FIFOs, ...)

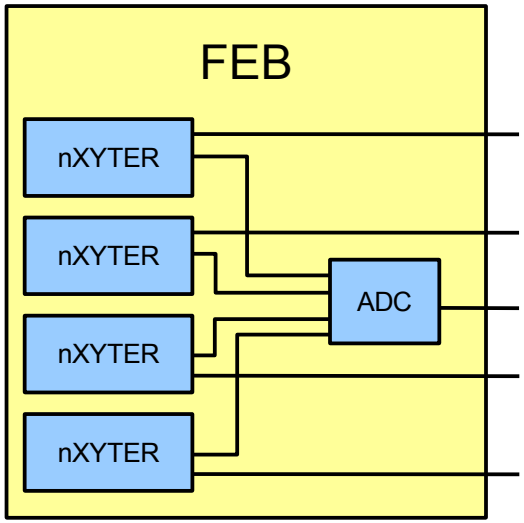
Synchronisation between chips

- The time stamp precision of 1ns results in a counter frequency of 1GHz.
- Time stamp requires precise global reset.
- Possible realizations:
  - The serial I/O building block from Brüning/Tielert should provide a precise reset output.
  - Simpler:
    - send reset which may not reach chips 'simultaneously', but which is stable
    - sent test injections to verify
    - cross – calibrate test injection to beam data



Benefit: ADC on chip

n-XYTER:
One ADC per n chips



Basic choice - three options with ADC(s) on chip:

- One ADC per chip: 128 x 250kHz → > 32Msamples/s
  - Available from Kaiserslautern (Tielert / Muthers)
  - Analog FIFOs are still needed
  - Crossbar between FIFOs and ADC (e.g. TR)
- One ADC per channel: Slower ADCs with 250kHz plus overhead would make it (500k-2MHz ADCs)
  - Double buffered input: No analog FIFOs needed
  - All data is early in digital domain; connection network can easier be realized
  - But the utilisation per ADC is small
- One ADC per n channels:
  - Hit distribution per n channels is better than only per channel; higher ADC utilisation
  - Less ADC sample speed overhead
  - Crossbar (TR) and FIFOs can be less complex
  - Compromise between first two options

Building Blocks

- Charge Amplifier
- Leakage current compensation
- Injection circuitry (fast digital, variable analog, arbitrary patterns)
- Fast Shaper / Time walk compensation / Discriminator / Trim
- Slow shaper / peak an hold (triggered by hit)
- Neighbour logic (?)
- Time base counter, clock generator (PLL, or from IO block)
- Analog / Digital FIFO
- Crossbar to ADC
- ADC
- Priority Scan
- Fast Serial Data Output
- Slow Control (I2C, JTAG), DACs, Reference

Specifications

- Must nail down more specifications soon to chose between options:

- Sensor parameters – for analog part
- Resolution requirements – for timing & ADC
- data rates & format – for R/O
- chip geometry / interconnect – for floorplan
- technology – to get started

Thank you for your attention!