A Self Triggered Amplifier/Digitizer Chip for CBM

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Introduction

The development of front-end electronics for the planned CBM experiment at FAIR/GSI is in full progress. For charge readout of the various sub-detectors a new self triggered amplification and digitization chip is being designed and tested.

The chip will have 32-64 channels each containing a low power/low noise preamplifier/shaper front-end, an 8-9 Bit ADC and a digital post-processing based on a simple FIR-filter. The ADC has a pipelined architecture that uses a novel current-mode storage cell as a basic building block.

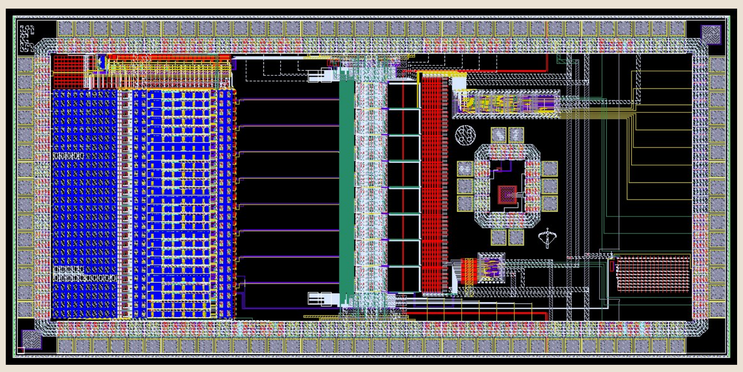
The current prototype provides 26 different parameterized preamplifier/shaper/discriminator channels, 8 pipelined ADCs, a readout shift register matrix built of 3T D-RAM cells and a synthesized redundant signed binary (RSD) decoder.

Basic Parameters of the Prototype

Chip Technology	UMC 0.18 µm, 1P6M, MiMCaps
Chip Area	1.5 × 3.2 mm²
Area of Channel / ADC	40 × 540 / 130 × 120 µm²
Number of Channels / ADCs	26 / 8
Power per Channel / ADC	3.8 / 4.5 mW
Shaper Noise (ENC)	800 e @ 30 pF (best channel)
Shaper Rise-Time	95 ns
ADC Resolution	9 Bit design, 7-8 Bit effective
ADC Speed	24 MSamples/s

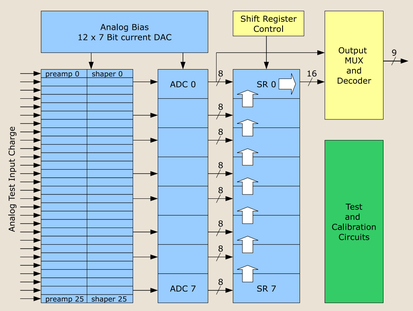
Layout of analog parts done by hand, two blocks were synthesized.

Prototype Layout



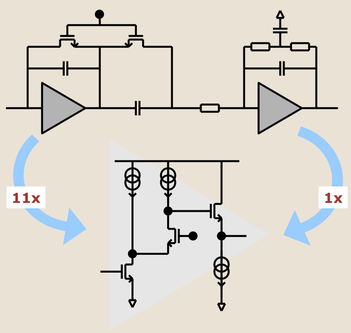
Prototype Architecture

Overview



The current prototype design is 2x1 Mini@sic blocks (3.2 x 1.5 mm²) large and has been fabricated in the UMC018 1P6M technology. One die carries 26 charge sensitive amplifier channels, 8 pipelined ADCs, a shift register matrix of 5.3 kBit, two synthesized control/decoder blocks and different test and calibration circuits.

Amplifier/Shaper Channels



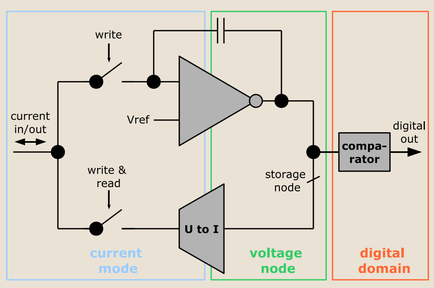
As shown left, each amplifier channel basically consists of a single-ended preamplifier with N-MOS input and a pole-zero cancellation feedback, a 2nd order T-feedback shaper (82 ns shaping-time) and a comparator (not shown) with LVDS output. The preamplifiers of the different channels were realized with varied design parameters to figure out what the lowest possible noise values are and how they can be achieved.

For both, preamplifier and shaper, a unified amplifier cell is used several times. Furthermore a special injection cell is included in every channel that provides 3 different ways for injecting test charges. The whole channel block was layouted by hand and covers about 40 x 540 µm².

Pipelined ADC

The current-mode pipelined ADCs have 8 pipeline stages and therefore generate 9 Bit per conversion step at a maximum speed of 24 MSamples/s. Each ADC produces a raw data stream of 400 MBit/s that is fed into the storage matrix. During ADC processing values older than 40 cycles are continuously discarded. In readout mode, by connecting the shift registers of all ADCs in series, the last 40 ADC values of each ADC are transferred to the RSD decoder where they are passed further to the outer world.

A sophisticated current storage cell, as sketched right, is used for both signal copying and offset correction - processes that are needed within the algorithmic working principle.

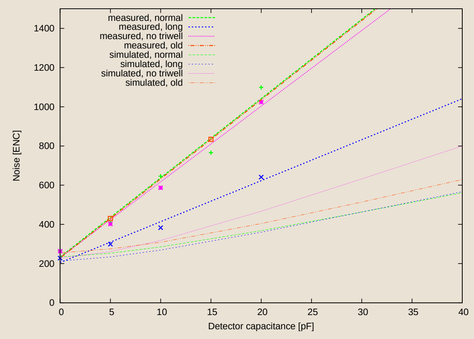


The basic idea of the current cell is to integrate the input current while concurrently reconverting the integator's output voltage back to a current, that is subtracted from the primary input current, until both currents exactly cancel each other.

Prototype Results

Preamplifier and 2nd Order Shaper

Well-known test charges can easily be injected into the amplifier inputs by using a calibrated internal injection capacitance. The pulse shapes of both the preamplifier and the shaper outputs can be studied qualitatively with a monitor bus, for precise noise values the discriminators are used to perform s-curve scans.



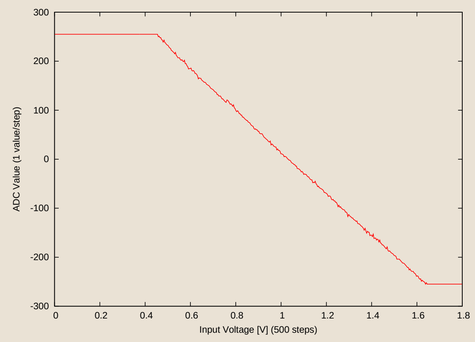
The overall pulse shapes and the general amplifier behavior matches nearly perfectly the simulation, whereas, as shown in the graphic above, the measured noise does not. Although the noise offset (at 0 pF detector capacitance) is for all simulations and measurements at about 200 e ENC, the measured slopes of the different channel versions differ significantly from both simulation and each other.

The most important result here is that hardly any parameter variation (input N-MOS with and without triwell, many minor layout and schematic refinements) did have a real impact on the measured noise, whereas using a longer input N-MOS (320nm instead of 180nm) caused a dramatic decrease of the noise slope by a factor of about 2. Neither this nor the absolute deviation of all noise values from simulation is really understood yet.

Nevertheless the “long” channel has a measured noise of 800 e ENC for a 30 pF detector capacitance while consuming only 3.6 mW and therewith already satisfies the project requirements.

Pipelined ADC

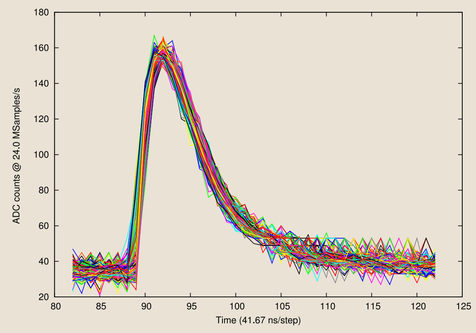
The ADC transfer characteristic has been measured with a dc input at a conversion speed of 24 MSamples/s and a clock frequency of 200 MHz, one exemplary result is shown below.



This measurement implicitly proves the proper operation of all readout components (shift register matrix, control blocks, redundant signed binary decoder, ...) and of the ADC itself.

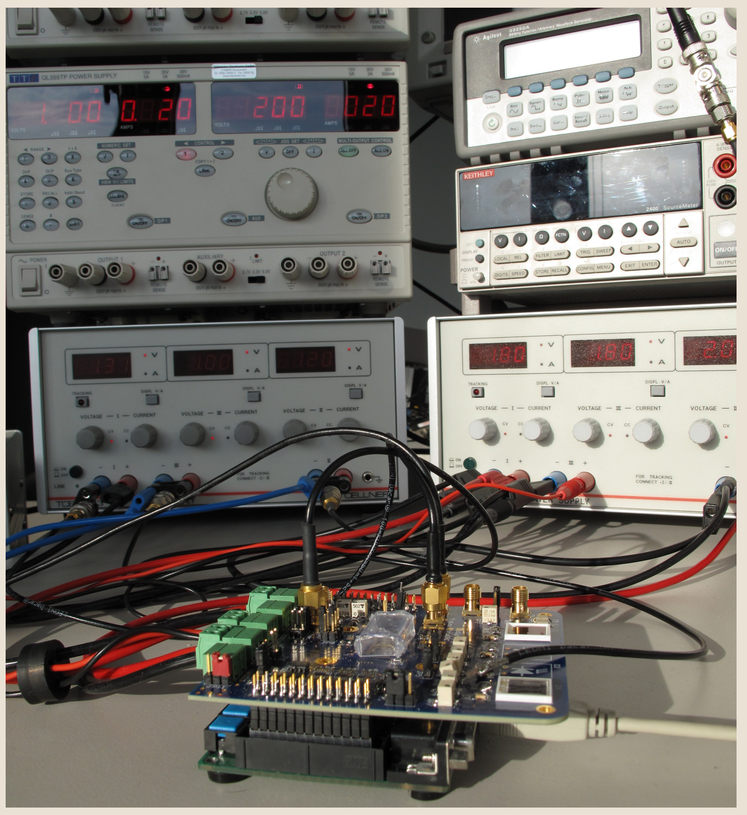
The best measurement of the 9 Bit design so far gives an effective resolution of 7-8 Bit while consuming 4.5 mW at 24 MSamples/s and covering only 130 x 120 µm² chip area.

System: Amplifier + ADC



The shaper pulses can be digitized by connecting an amplifier output to an ADC. Since the readout must be triggered internally or externally, the whole system then just acts like an oscilloscope. For the upper plot 1000 hits were recorded in this way. Since the shaper noise is smaller than one LSB (@ 5pF input load) of the ADC, the observable disturbance here is only caused by ADC noise.

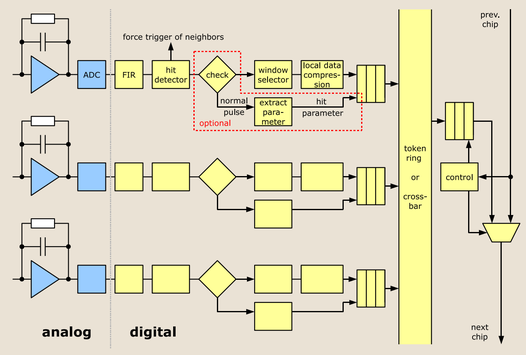
Test Setup



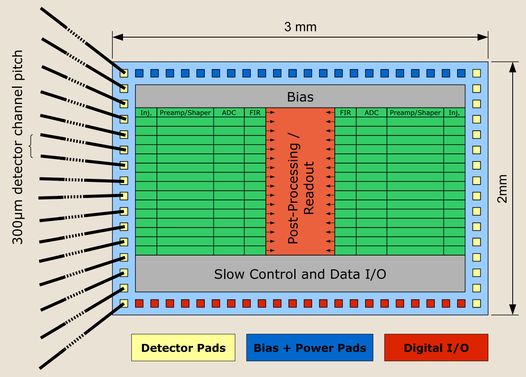
The prototype chip is directly bonded to a PCB that also carries the bias circuitry, some LVDS buffers, level shifters and different connectors. The PCB is mounted on a self-made Xilinx Spartan FPGA board that provides the necessary infrastructure for FPGA programming and data exchange via USB with a PC.

Outlook: CBM Readout Chip V1.0

The next milestone is to build a complete V1.0 ASIC that has 32 analog channels, each consisting of an amplifier, an ADC and a post-processing unit based on a FIR-filter. Moreover some digital post-processing units (e.g. a simple data compression) and a 1-2 GBit LVDS transmitter including a protocol encoder are intended. A very first draft of the block diagram is shown below.



To save transmission bandwidth it is intended to connect several chips with lower load (due to a lower event rate) to enable them to share one LVDS transmitter. An hit parameter extraction unit that evaluates information like hit amplitude or time-stamp is currently in discussion. To connect the channel outputs to the digital processing unit a token ring network seems to be the most simple and evenhanded solution.



The basic floorplan concept is shown in the graphic above. The placement and power routing structure should already have a final character. The submission is scheduled for end of 2010.